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LOW POWER AND AREA EFFICIENT TEST PATTERN GENERATION FOR BIST USING RING COUNTER

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Abstract: - This paper presents architecture to generate the test patterns for Built-in-self-test (BIST) that varies in single bit position. The Multiple single input change (MSIC) test patterns generated by using reconfigurable Johnson counter and linear feedback shift register (LFSR) lack interrelation between consecutive test vectors and consume more area and power. So, in order to reduce the overall area and power consumed while generating the test patterns, the patterns are generated by using ring counter and accumulator architecture with carry select adder (CSA). Due to the single bit change between the consecutive test vectors, less power is consumed. Moreover, the area occupied by the proposed methodology is diminished. Simulation results shows a reduction of 43.9% in area and 57% in power when compared to the pattern generation using reconfigurable Johnson counter and LFSR. The methodology for test pattern generation for BIST is coded in Verilog and simulations, area and power report are obtained with the help of Xilinx 14.5.

Keywords: Built-in-self-test (BIST), multiple single input changes (MSIC), linear feedback shift registers (LFSR), Test pattern generator (TPG), carry select adder (CSA)

1. Introduction

Testing is required as it verifies the correctness of hardware. Every circuit has to be tested before it is shipped out to the market because the chip manufacturing process cannot provide 100% yield. The testing performed by using Automatic test equipment (ATE) requires larger time and is expensive. To overcome these problems, BIST technique is introduced. BIST is a design for testability (DFT) technique in which an additional circuitry is placed on the chip to facilitate testing. Testing can be done at normal operating speed. BIST techniques are classified as online BIST and offline BIST. In online BIST, the testing is carried out during the interval when normal operation occurs. In offline BIST, the testing is carried out when the circuit is idle. The test patterns are applied to the circuit under test(CUT) in order to determine the fault by comparing the actual responses with the expected responses. The main advantages of BIST over ATE are lower cost of test, better fault coverage, shorter test time and the testing can be performed throughout the operational life of the chip. Test pattern generation for BIST schemes can be divided into three categories namely exhaustive testing, pseudo exhaustive testing and pseudorandom testing. The exhaustive testing technique can detect all the non-redundant faults. But, the drawback is it takes longer test times. A modified form of exhaustive testing is pseudo exhaustive testing in which each circuit is divided into parts and each segment is exhaustively tested. In pseudorandom testing, the patterns are generated to reduce the test length reducing the time for testing.

A circuit consumes more power in test mode than in normal mode. This extra power consumption can gives rise to severe hazards in circuit reliability. Moreover, it creates problems such as increased product cost,

difficulty in performance verification and decrease of overall yield. Low power dissipation during test application is becoming increasingly important in VLSI systems design and is a major goal in future development of VLSI design.

P. Girard in [2], discussed the reasons and consequences of increased power during test and proposed various techniques for low power testing for VLSI circuits. A. Abu Issa and S. Quigley presented a bit swapping LFSR(BS-LFSR) which can generate test patterns for scan based BIST to reduce the number of transitions in the scan chain ordering. In [3], P. Girard et al. proposed a low power BIST design based on simulated annealing algorithm. S. Wang and K. Gupta in [4] proposed a Dual speed LFSR which has a slow LFSR and a normal speed LFSR operating at different frequencies in order to reduce the switching activity in test application. P. Girard et al. in [5], modified the clock pulse for reducing the power.

For testing the data paths, D. Gizopoulos proposed a methodology for producing deterministic patterns. In [6], C. Laoudias proposed a new test pattern generator (TPG) for low power test sequences with high defect efficiency. S. Bhunia et al. presented a technique of masking signal transitions by inserting an extra gating transistor in the supply to ground path in order to reduce the power dissipation. X. kavousianos in [7], proposed a suitable method for gating subset of scan cells for reducing the dynamic power dissipation during scan based testing. In [8], M. Nandini priya presented a test pattern generator using Johnson counter and accumulator in order to achieve area reduction.

The rest of the paper is organized as follows. In section II, the existing methodologies are presented. In section III, the proposed methodology is presented. In section IV, the simulation results and analysis are discussed. Finally, the conclusion is given in section V.

2. Existing Methodologies

The test patterns for BIST can be generated by MSIC-TPG using test per clock scheme or an architecture consisting of a Gray counter, Decoder and accumulator. The test vectors generated are applied to the multiplier circuit and faults are detected by comparing the response of the circuit with the expected response.

2.1 Pattern Generation

The pattern generation method for MSIC vectors uses reconfigurable Johnson counter, seed vector and x-or operation. For every clock pulse, the reconfigurable Johnson counter generates the Johnson vector and the Linear feedback shift register generates a seed [9]. The Exclusive-or operations are done between Johnson counter and the seed vector in order to produce the test patterns. These produced vectors are shifted in to scan chains [9].

In the next clock pulse, the Johnson vectors will be circularly shifted and will bit-xor with seed. The resulted test patterns will be shifted in to the scan chains. The procedure is repeated until all the scan cells are loaded. Finally, the generated test vectors will be applied to the 4*4 multiplier circuit.

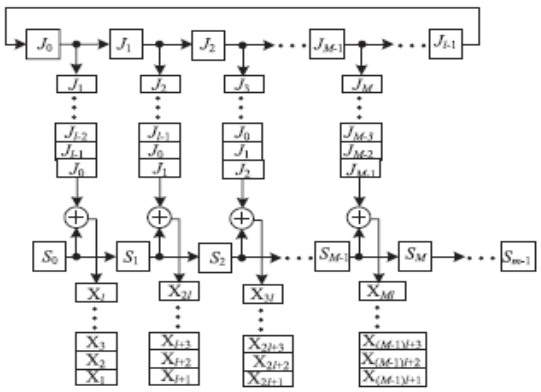

Fig 1. Test pattern Generation

2.2 Reconfigurable Johnson counter

The three different modes of operation for reconfigurable Johnson counter are initialization mode, circular shift mode and normal mode. Reconfigurable Johnson counter is constructed by using AND gate, a multiplexer and eight delay flip flops.

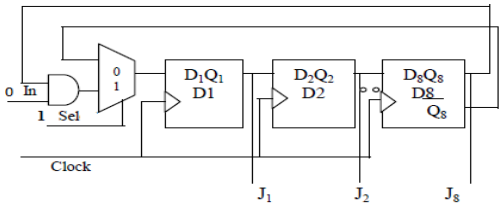

Fig 2. Initialization mode

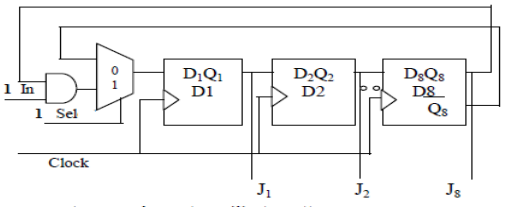

Fig 3. Circular shift mode

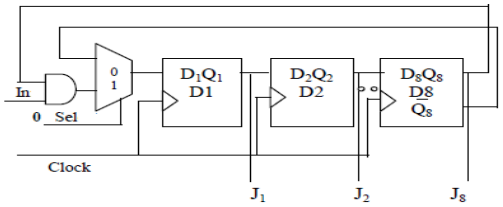

Fig 4. Normal mode

In initialization mode as shown in the fig 2, the reconfigurable Johnson counter will be initialized to all zero states by keeping 'sel' input of multiplexer at a value 1. In circular shift mode, the 'sel' input is made 1 and the input to the AND gate 'in' is made 1 by which the output Q8 is feedback as shown in the fig 3. To operate the reconfigurable Johnson counter in normal mode as shown in the fig 4, the 'sel' input of multiplexer is made 0 by which the inverted output of the last delay flip flop will be feedback.

2.3 TPG using test per clock

The outputs of the Johnson counter and seed generator are applied to the x-or gate to produce the test patterns. The clock and control circuit produces the clk1 and clk2 signals. The clk1 and clk2 are applied to the seed generator and Johnson counter respectively in order to produce the seed and Johnson vectors.

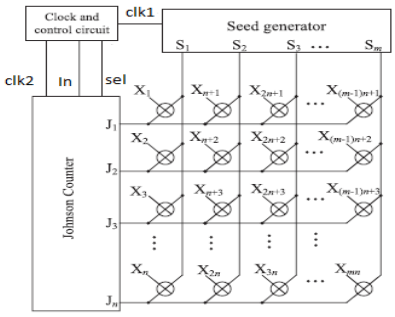

Fig 5. Pattern generation

The procedure for pattern generation is as follows

1. By applying clk1 to seed generator, the seed is produced.
2. A new Johnson vector is produced every time by clocking clk2.
3. By repeating 2, 2*l* Johnson vectors are generated.
4. For expected fault coverage, the steps 1-3 are repeated.

2.4 TPG using Gray counter

The test pattern generation using Gray counter, Decoder and accumulator architecture is shown in fig 6.

The purpose of using gray counter is to prevent the unwanted signal transition at the input. As the patterns produced by the gray code counter has only single bit change between the subsequent test vectors, power optimization can be achieved. For every clock pulse, a 4- bit gray code is applied to the 3 to 8 decoder. The output of decoder is applied to the register B. The set and reset inputs are given to the registers in order to store the result. The outputs of two registers are given to a ripple carry adder and the final output test patterns are obtained from register A.

The produced patterns are applied to the 4*4 multiplier circuit and the response obtained is compared with the forecasted result to verify the functioning of the circuit.

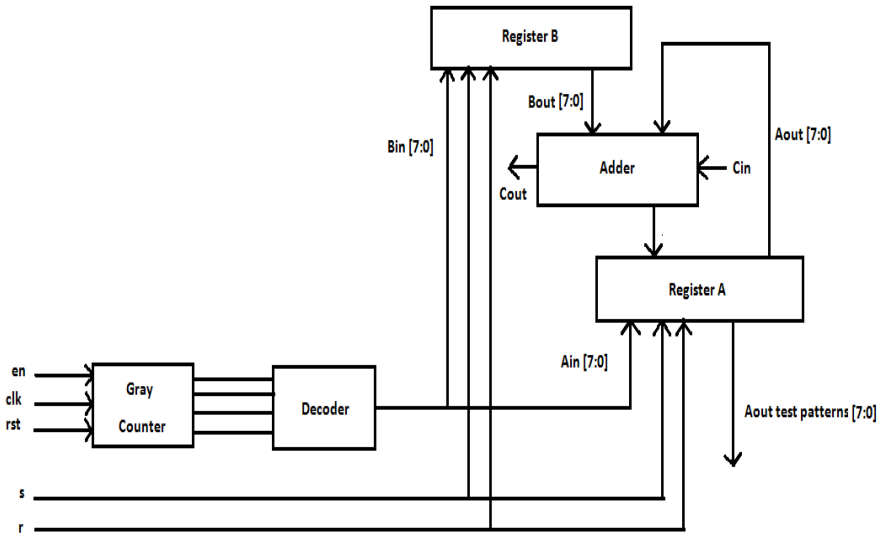

Fig 6. TPG using Gray counter

3. Proposed Methodology

The proposed methodology for test pattern generation is designed by using an 8-bit ring counter and accumulator architecture with carry select adder as shown in the fig 7.

For every clock cycle, the ring counter produces an 8-bit pattern. The generated pattern is applied to the register B. Initially, the register A has zero state. The pattern presented in the register B is stored in register A. For the next clock cycle, the new test vector produced by the ring counter is added with the previously stored result in register A thereby producing a single bit change between the consecutive test vectors. The generated patterns are tested on the 4*4 multiplier circuit.

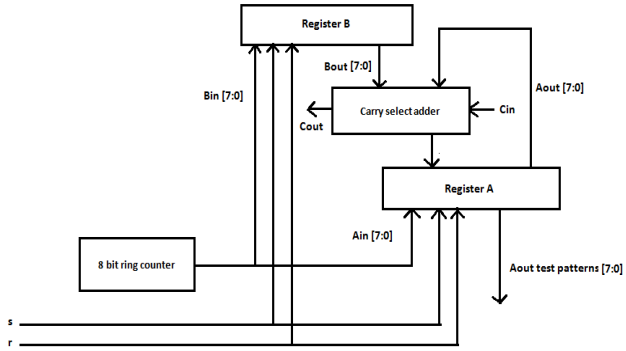

Fig 7. TPG using ring counter and Accumulator with CSA

The proposed architecture of TPG using ring counter and accumulator with carry select adder has an advantage of area optimization. The sequence of patterns produced has a single bit change reducing the requirement of power.

4. Simulation results & Comparison

The test pattern generation for BIST using different methodologies is coded in Verilog and implemented using Xilinx ISE 14.5 software. When clk2 is clocked, the reconfigurable Johnson counter generates a Johnson vector and seed generator produces a seed '01101' thereby producing the test patterns which are applied to test the 4*4 multiplier circuit.

The simulation results for TPG and testing of multiplier using reconfigurable Johnson counter and LFSR is shown in fig 8 and fig 9 respectively. This TPG requires 41 no. LUTs and consumes 82 mW of power.

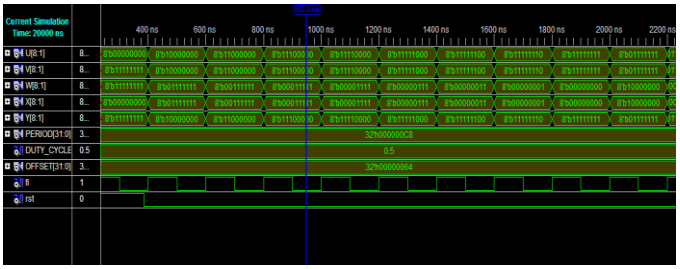

Fig 8. Test pattern generation using reconfigurable Johnson counter and LFSR

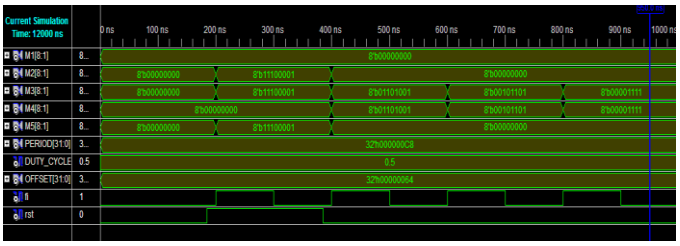

Fig 9. Testing of multiplier using the TPG produced by reconfigurable Johnson counter and LFSR

The test pattern generation using gray counter and accumulator exhibits a single bit change between the consecutive test vectors reducing the unwanted power dissipation. These generated patterns are applied to the 4*4 multiplier circuit. The simulation results for TPG using gray counter & accumulator and the testing of multiplier using these patterns are shown in fig 10 and fig 11 respectively.

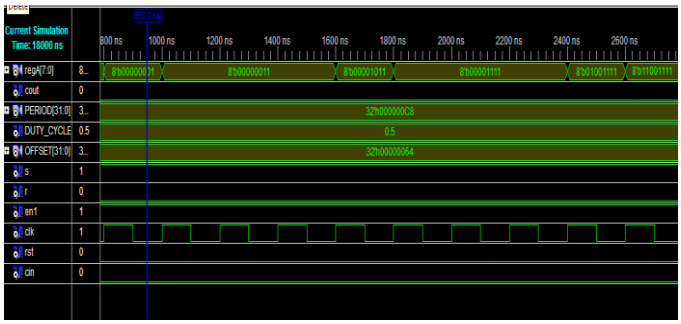

Fig 10. Test pattern generation using gray counter and accumulator architecture

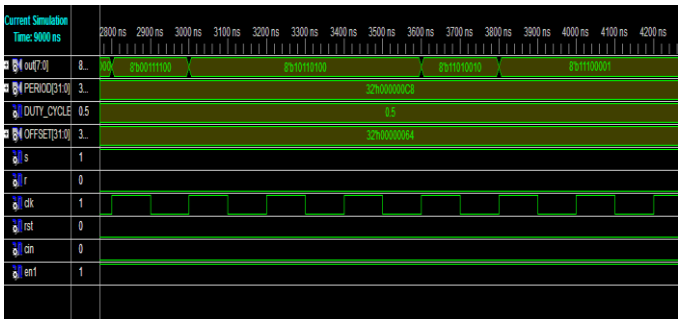

Fig 11. Testing of multiplier using the TPG produced by using gray counter and accumulator

The test patterns generated by the proposed methodology using 8-bit ring counter and accumulator architecture produces the patterns with single bit change between the consecutive test vectors thereby reducing the area and power requirement when compared to the TPG using the existing methodologies.

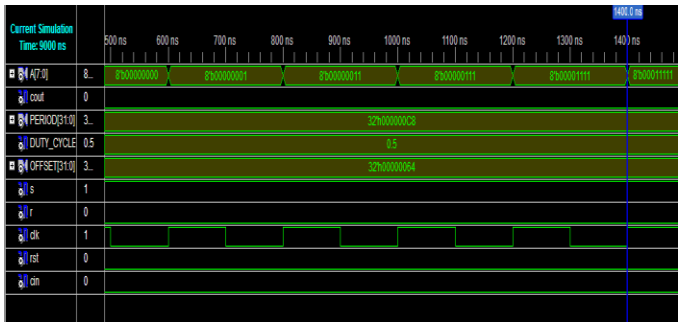

Fig 12. Test pattern generation using ring counter and accumulator with CSA

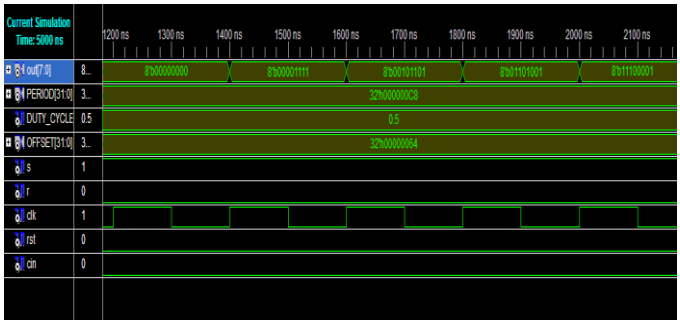

Fig 13. Testing of multiplier using the TPG produced by ring counter and accumulator with CSA

	Area (no of LUTs)	Power (mW)	Delay (ns)
Reconfigurable Johnson counter and LFSR	41	82	5.29
Gray counter, Decoder and Accumulator	39	37	9.84
Ring counter and accumulator with CSA	23	35	10.67

Table: Comparison of power and area for different TPGs

5. Conclusion

The test patterns produced using ring counter and accumulator architecture achieves area and power optimization significantly. The proposed architecture produces single bit change between consecutive test vectors improves the correlation thereby reducing the power requirement. The methodology for generating the test patterns is coded in Verilog and simulated using Xilinx ISE 14.5. The area and power report is obtained using Xilinx ISE 14.5 software. The proposed methodology shows reduction of 43.9% in area and 57% in power requirement when compared to the TPG using reconfigurable Johnson counter and LFSR.

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