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CMOS DESIGN AND LOW POWER FULL ADDER USING .12 MICRON TECHNOLOGY

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Abstract
In this paper, we are presenting a 8T full adder using 1-bit consuming less power than a conventional adder using 24T.The main objective is to design that 8T circuit with low power consumption and due to its reduced transistor count, a very low power full adder is realized. The circuit is optimized at .12 micron CMOS technology .The conventional is compared to 8T Full adder based on power consumption, speed and power delay intensive simulation runs on microwind technology shows now 8T adder has 60-70% power saving over conventional one.
General Terms: 24T and 8T

Keywords: Full adder, Microwind simulator, VLSI circuit and low power.

1. INTRODUCTION

CMOS VLSI circuit is used for increasing no of portable application with limited amount of power available. VLSI design has been focusing high performance for microprocessor and system component. The research effort in low power microelectronic has been intensified demand in application such as personal computing device, wireless communication system. Medical application and other due to fast growth of battery operation all logic structure has a single-bit full adder as a main component in it. Adder cell effect the performance of logic structure most.

By running digital circuit in threshold mode we could get ultra-low power.

When the gate source voltage(V_{gs}) of MOSFET transistor become lower than threshold voltage(V_{th}) the sub-threshold current occur to reduce the power consumption we reduce the supply voltage the drawback of reducing voltage increase the circuit delay. When V_{gs} become greater than V_{th} the gate area repel the majority carrier present in channel the minority carrier. This is known as “strong-inversion”in condition $V_{gs}<V_{th}$ the “weak-inversion” take place.

When in CMOS design Vth become greater than V_{dd}. The circuit can be operated using the sub-threshold current in ultra-low power consumption. The compared 8T circuit operates efficiently to achieve ultra-low power result shows improvement in power consumption over the conventional adder.

2. ADDER

An adder or summer is a digital circuit that performs addition of noise in many computers and other kinds of processors, adders are not only in arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar operations.

For many numerical representations it can be use, such as binary code decimal or excess-3.The most common adder operates on binary numbers in case where two's complement or one's complement is being used to represent negative numbers.

3. CONVENTIONAL FULL ADDER

It adds binary numbers and accounts for values carried in as well as out. A one bit full adder has 3 one-bit numbers A, B and C_{in}whereA &B are the operands and Cin is a bit carried it from the next less significant stage. The full adder is usually a component in a cascade of adders which add 8, 16, 32 bit.

SUM = 2*C_{out} + sum

S = A xor B xor C_{in}

C_{out} = (A. B) + (C_{in}(AxorB))

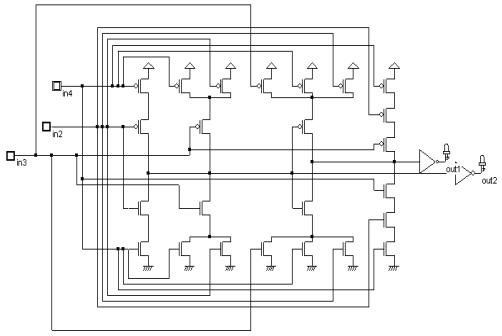

Fig.1Conventional Adder using 24 Transistor

Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig.2 Truth Table for Conventional Adder

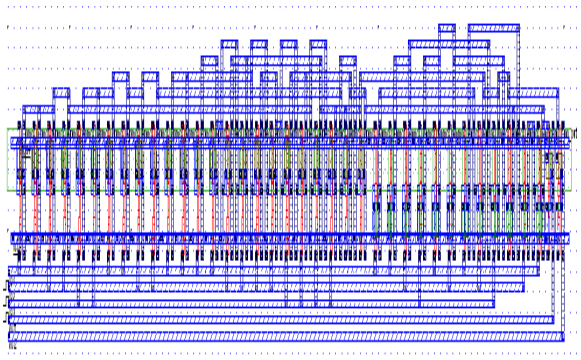

Fig.3 Microwind layout for Conventional Adder

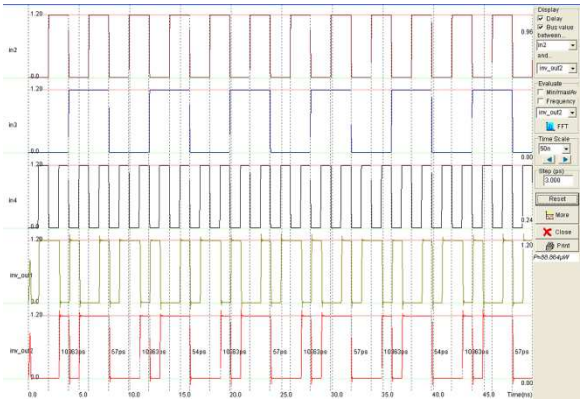

Fig.4 Voltage vs time output plot for Conventional Adder

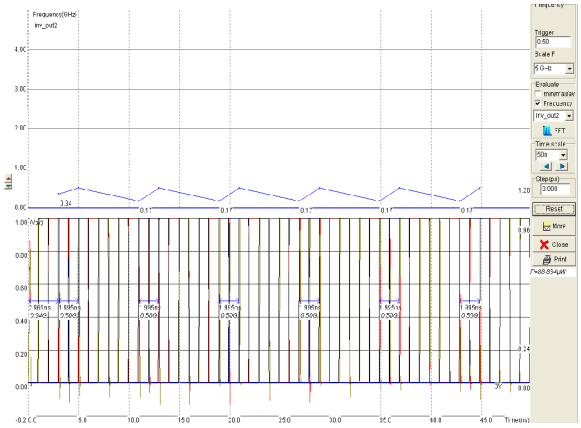

Fig.5 Frequency vs time output plot for Conventional Adder

The complementary CMOS full adder as shown in figure1.GeneratesCout throughout the single static CMOS gate. That is based on conventional pull-up and pull-down transistor. Weak-driver is formed at output stage by using

series transistor. Therefore, for providing the necessary driving power at cascade cells we required some additional buffer at the last stage. The main advantage of complementary CMOS is sensitive in nature against voltage scaling and transistor sizing.

4. FULL ADDER USING 8T

Figure 6 shows the 1-bit full adder cell using 8 transistor that can be implemented using different combination of xor modules and the multiplexer. In fig6 the sum output will occur at the end cascade connection of T4 and T6 and C_{out} we get at 2T multiplexer T7 and T8 from the fig we could see that for getting sum output and carry output the two stage delay required by increasing the aspect ratio we could minimize the voltage drop due to threshold loss in transistor T3 and T6.

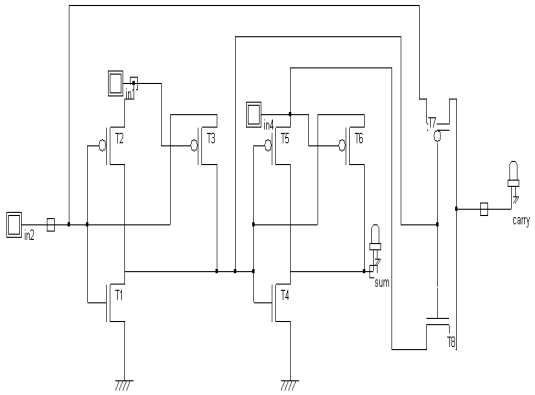

Fig.6 Adder using 8 Transistor

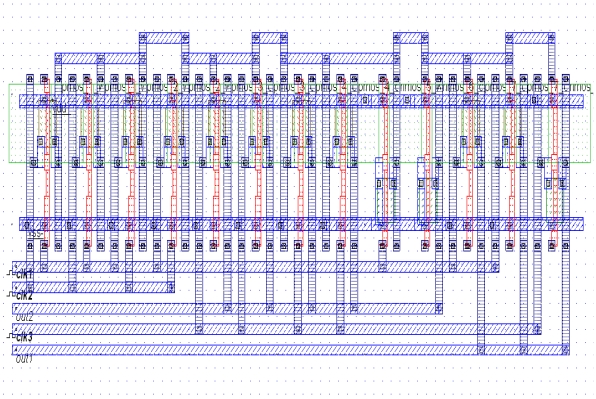

Fig.7Microwind layout for Adder for 8T

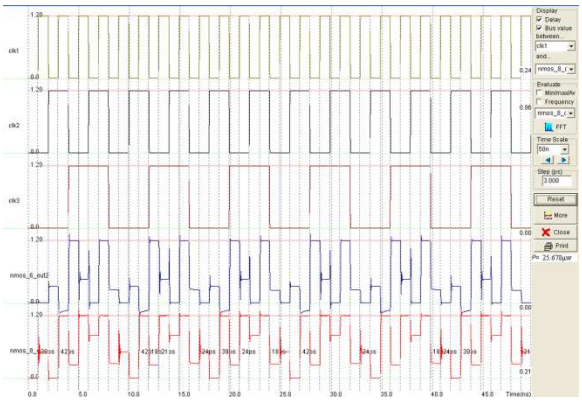

Fig.8Voltage vs time output plot for Adder using 8T

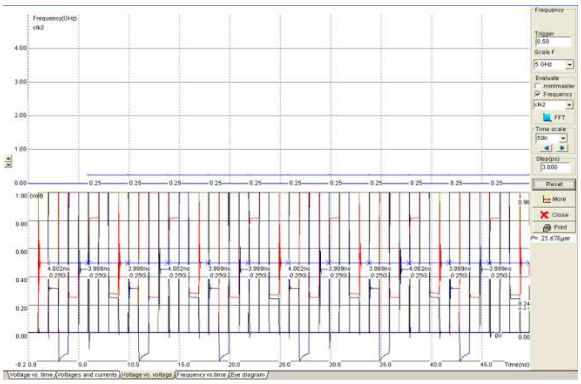

Fig.9 Frequency vs time output plot for Adder using 8T

For input '110' the output of first xor gate is '0' and when C_{in}=0,thiswill enable transistor T2 and M3 which gives a degraded sum output same output will remain same for input '000' similarly for input '100' sum should be '1' and C_{out} to be '0' in that condition due to degraded output at first xor gate however at higher input voltage the transistor T1 and T3 and T4 and T6 gets on simultaneously and output become much less in terms of power.

5. SIMULATION AND PERFORMANCE

We have performed simulation using microwind tool for CMOS designing at 120 nm technology in sub-threshold region the input voltage ranges from to for establishing a performance between both 24T and 8T which covers all the stream combination.

S. No.	PARAMETERS	Full Adder using 24T	Full Adder using 8T
1.	Propagation Sum Delay	1.135 ns	2.00 ns
	Carry	1.051ns	0.923ns
2.	Power Consumption	88.834µW	25.678µW
3.	Frequency Sum Content	881Mhz	500Mhz
	Carry	951Mhz	1083Mhz
4.	Layout Area	513.3µm^2	147.3 µm^2

5.	Capacitance	0.354fF	1.504fF
6.	Low Leakage Current	.203mA	0.993mA
7.	Low Leakage Threshold Voltage	0.40V	0.40V

Table I. Simulation Results of Full Adder using 24T and 8T.

6. CONCLUSION

The 8T 1-bit adder is better than the conventional one although it has some disadvantages but still power dissipation due to this is less than conventional one. The combination of better power delay threshold voltage .40 volt makes the 8T is a viable option for low power application.

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